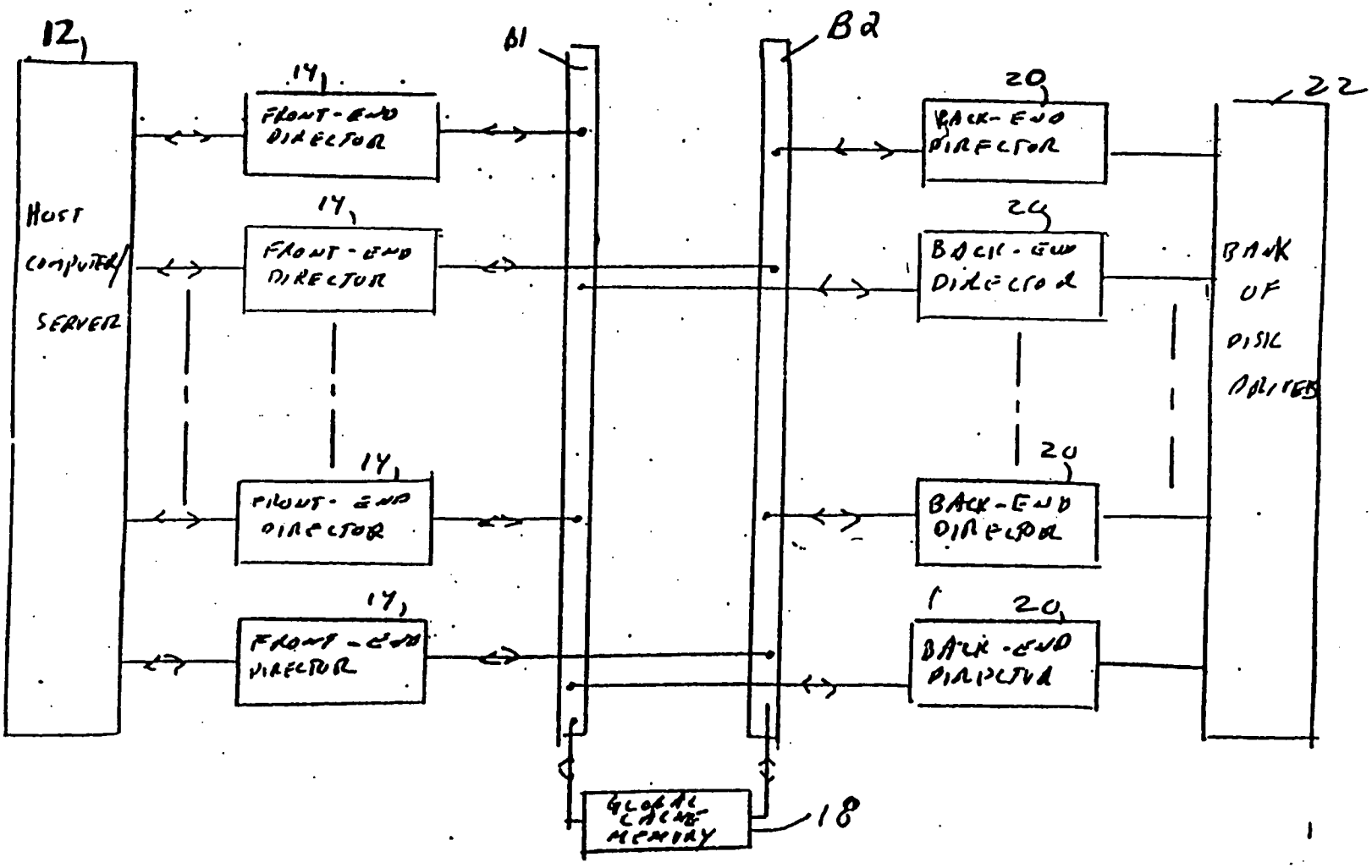
FIG. 1
PRIOR ART



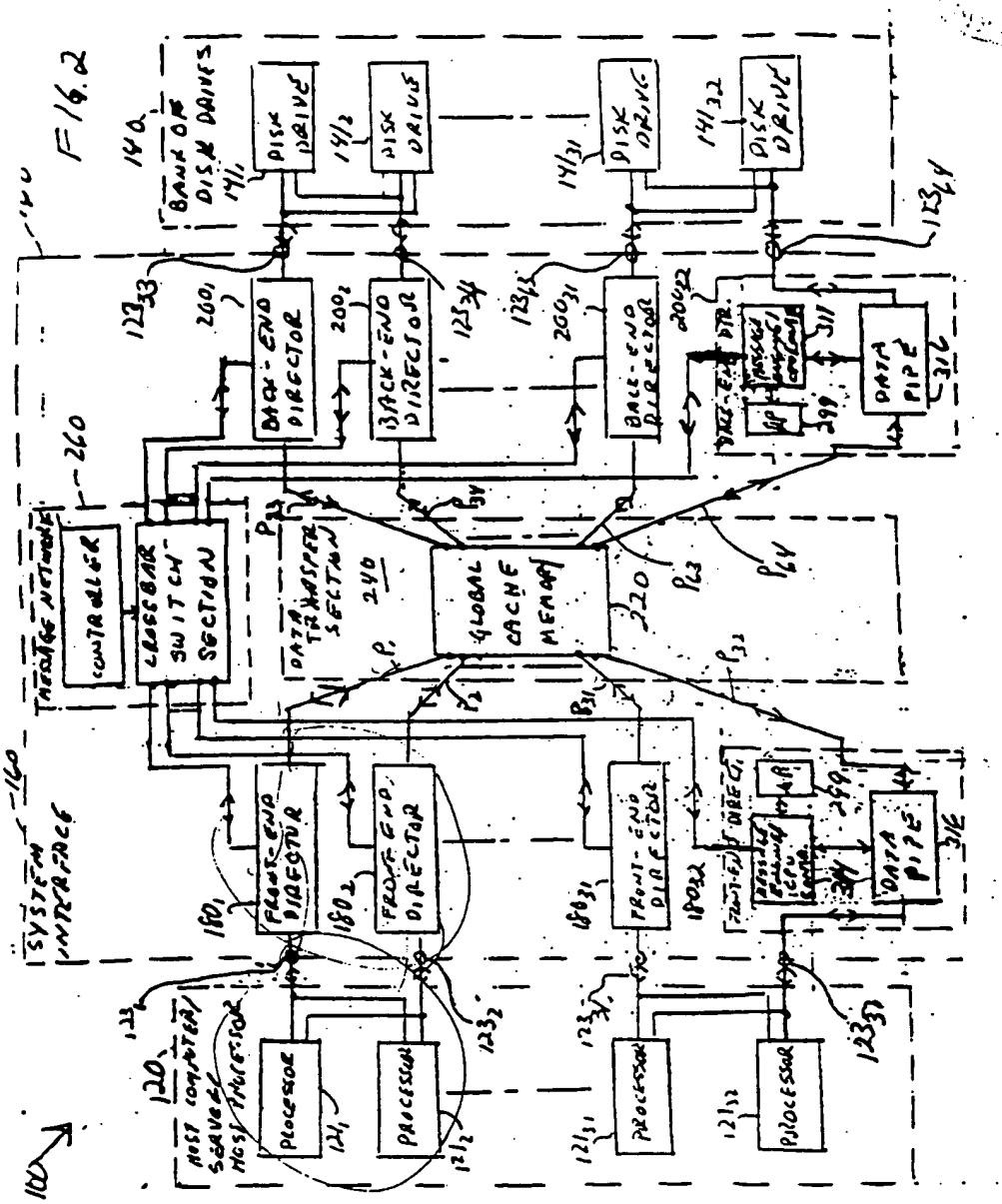


FIG. 2
100
120
140
141
160
180
200
220
240
260
280
300
310
316
320
DISK DRIVES
DISK DRIVE
SYSTEM INTERFACE
HOST COMPUTER/ SERVER/ HOST PROCESSOR
PROCESSOR
FRONT-END DIRECTOR
BACK-END DIRECTOR
GLOBAL CACHE MEMORY
DATA TRANSFER SECTION
CONTROL
CROSSBAR SWITCH
SECTION
DATA PIPE

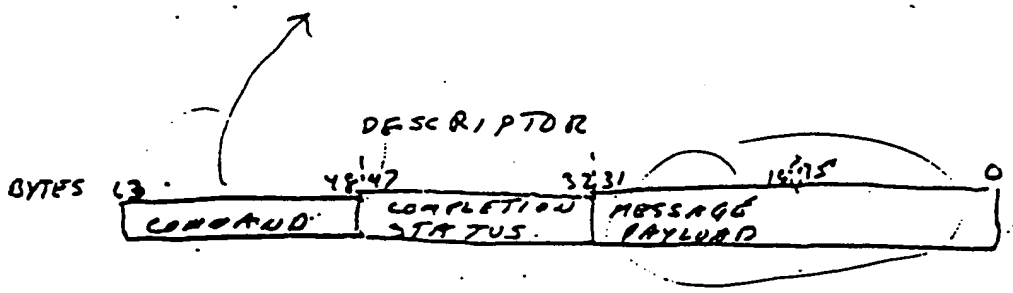

DESCRIPTOR
BYTES
63
48
47
32
31
16
15
0
COMMAND
COMPLETION STATUS
MESSAGE PAYLOAD

FIG 2A

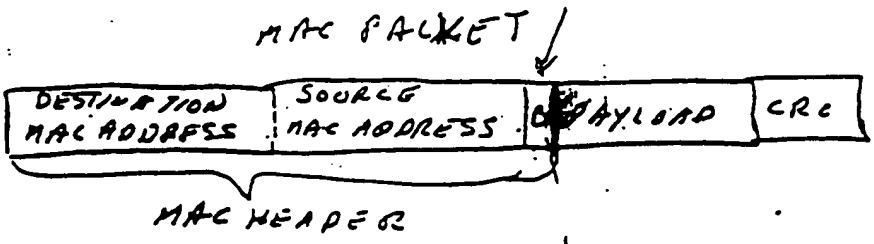

MAC PACKET
DESTINATION MAC ADDRESS
SOURCE MAC ADDRESS
PAYLOAD
CRC
MAC HEADER

FIG 2B

FIG. 3

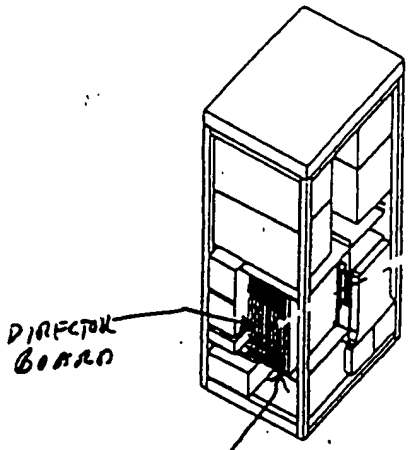
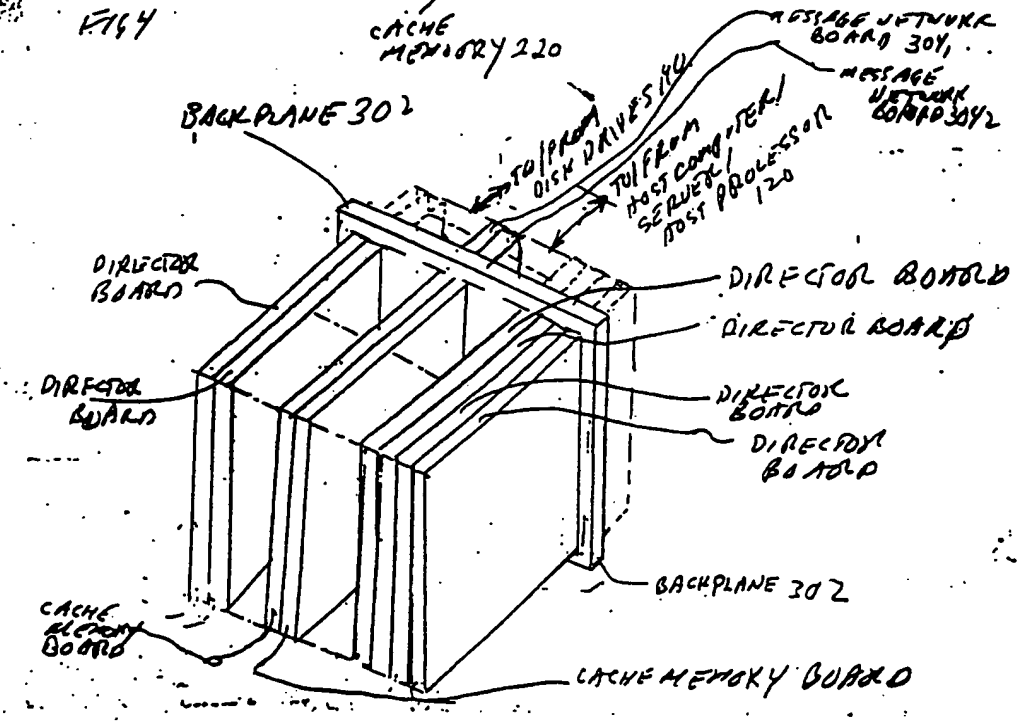
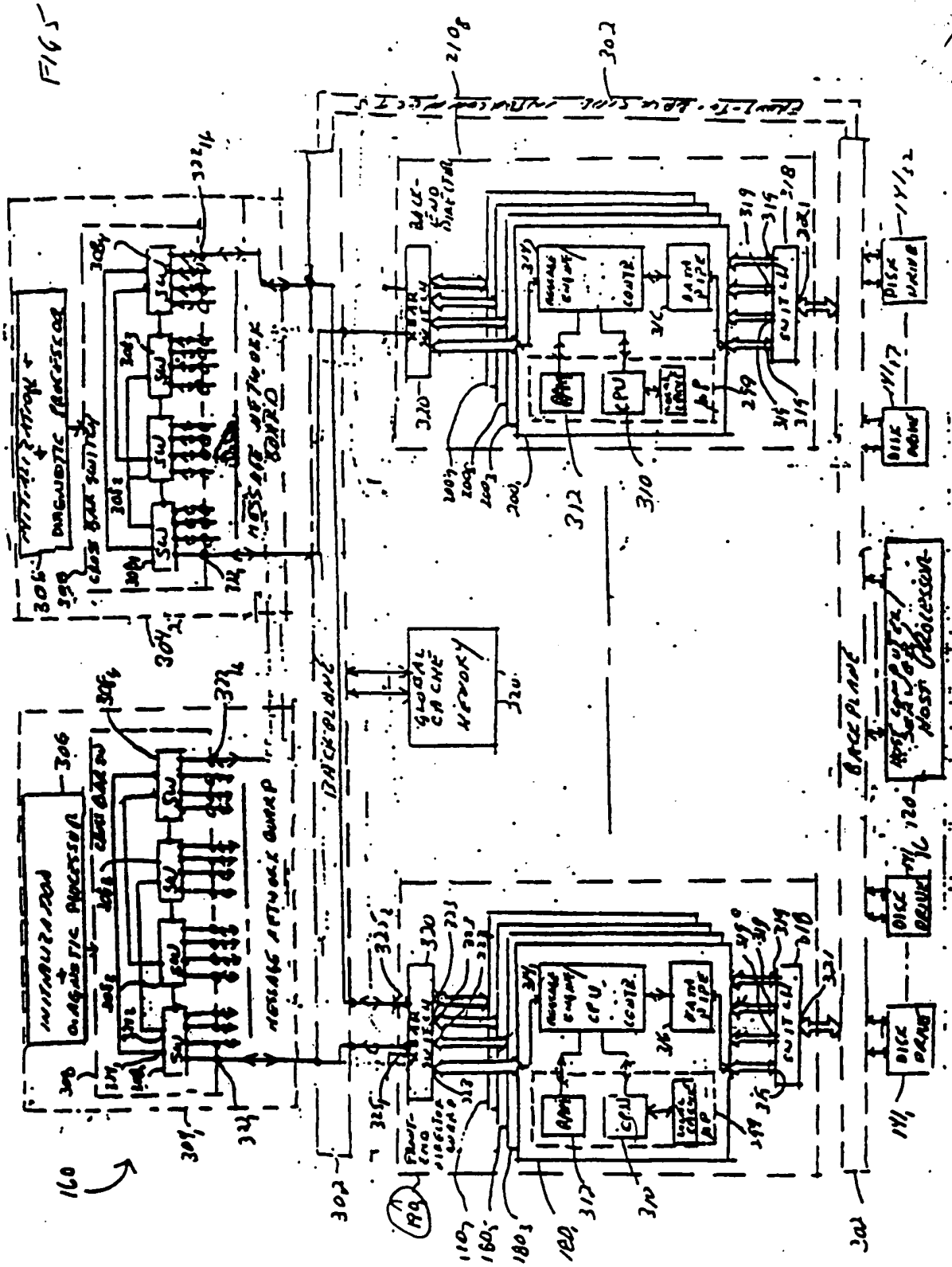
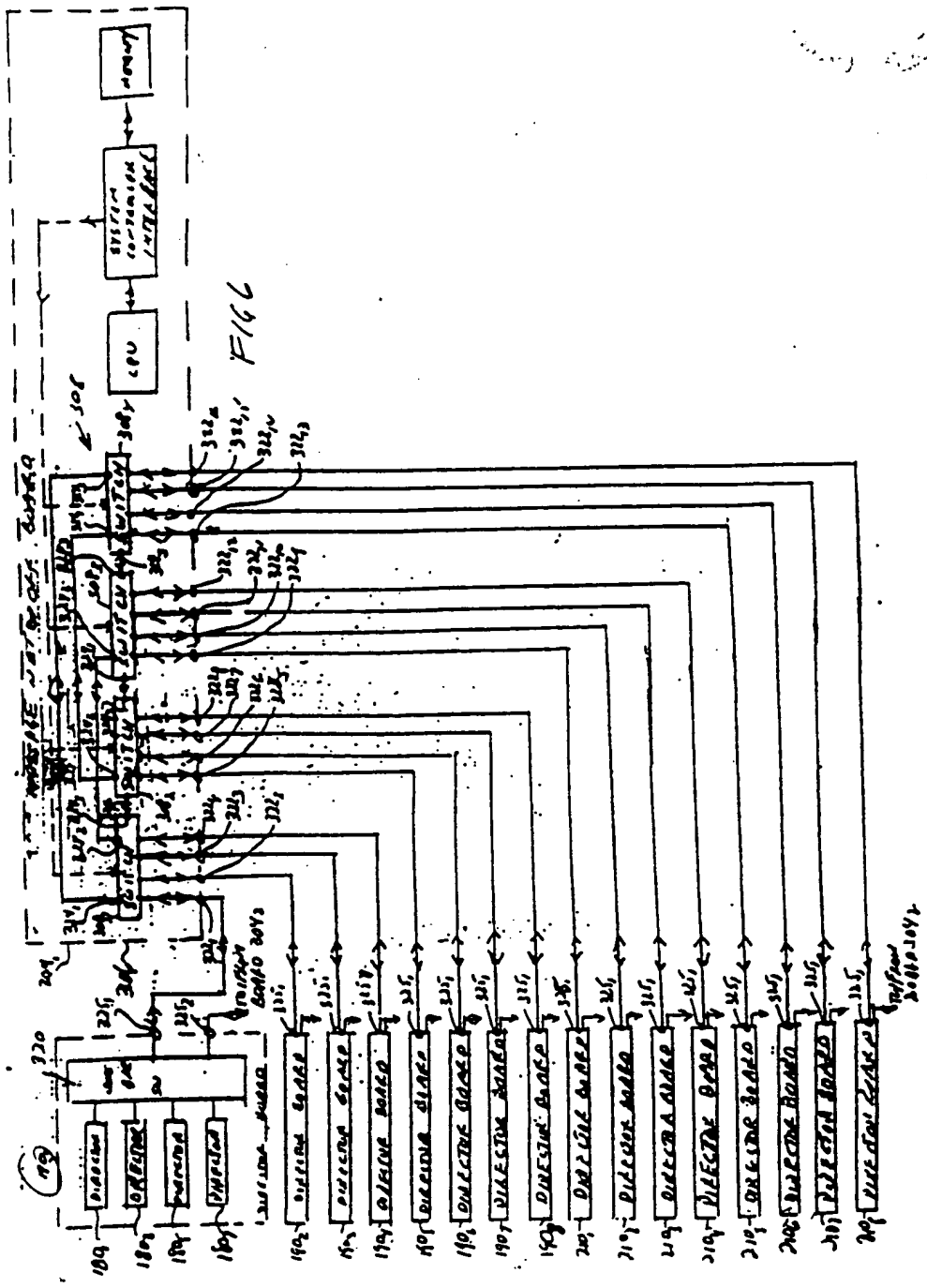

DIRECTOR BOARD
CACHE MEMORY 220

FIG 4


BACKPLANE 302
TO/FROM DISK DRIVES 114
TO/FROM HOST COMPUTER/ SERVER/ HOST PROCESSOR 120
MESSAGE NETWORK BOARD 304
MESSAGE NETWORK BOARD 304
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD





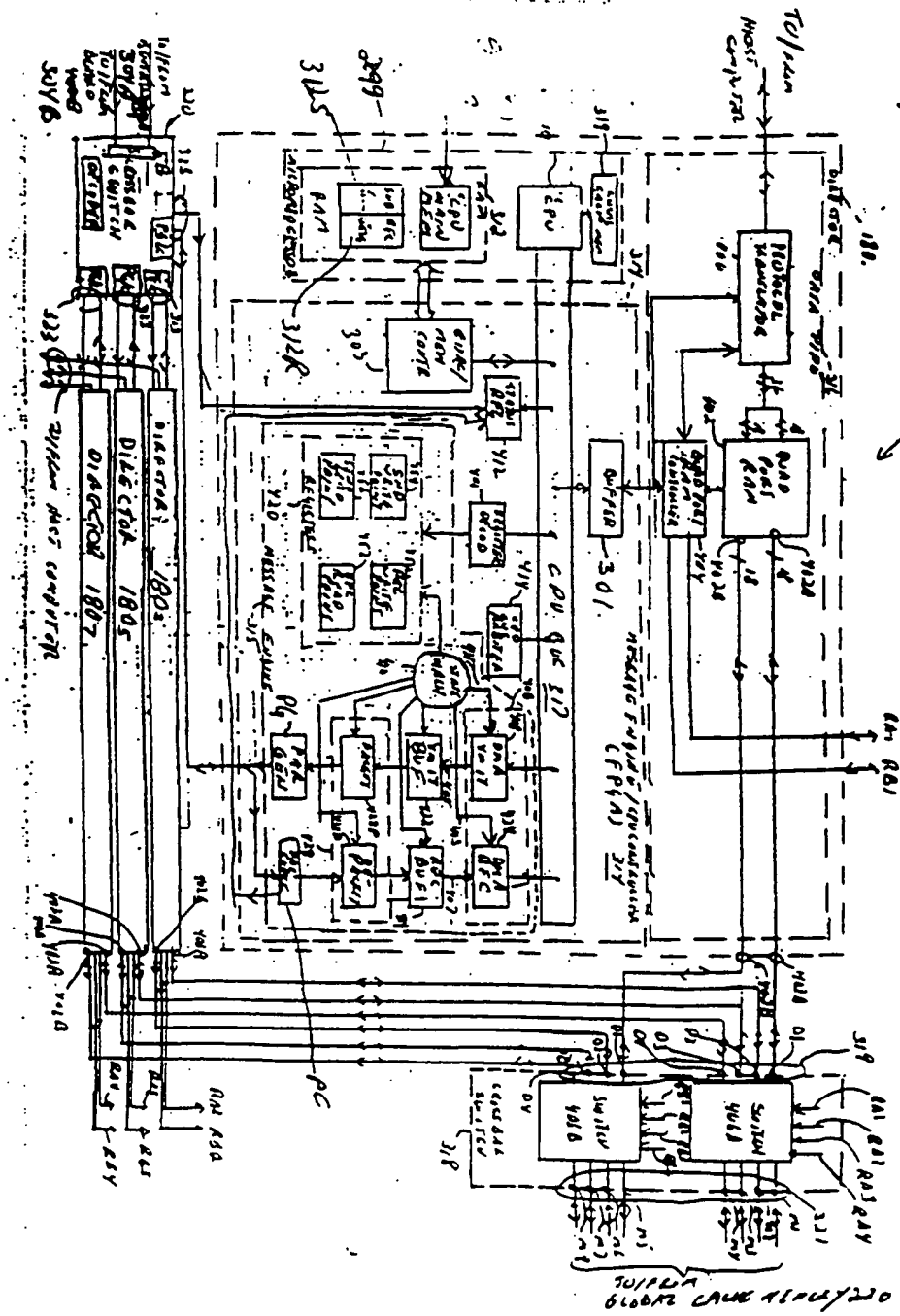


FIG. 7

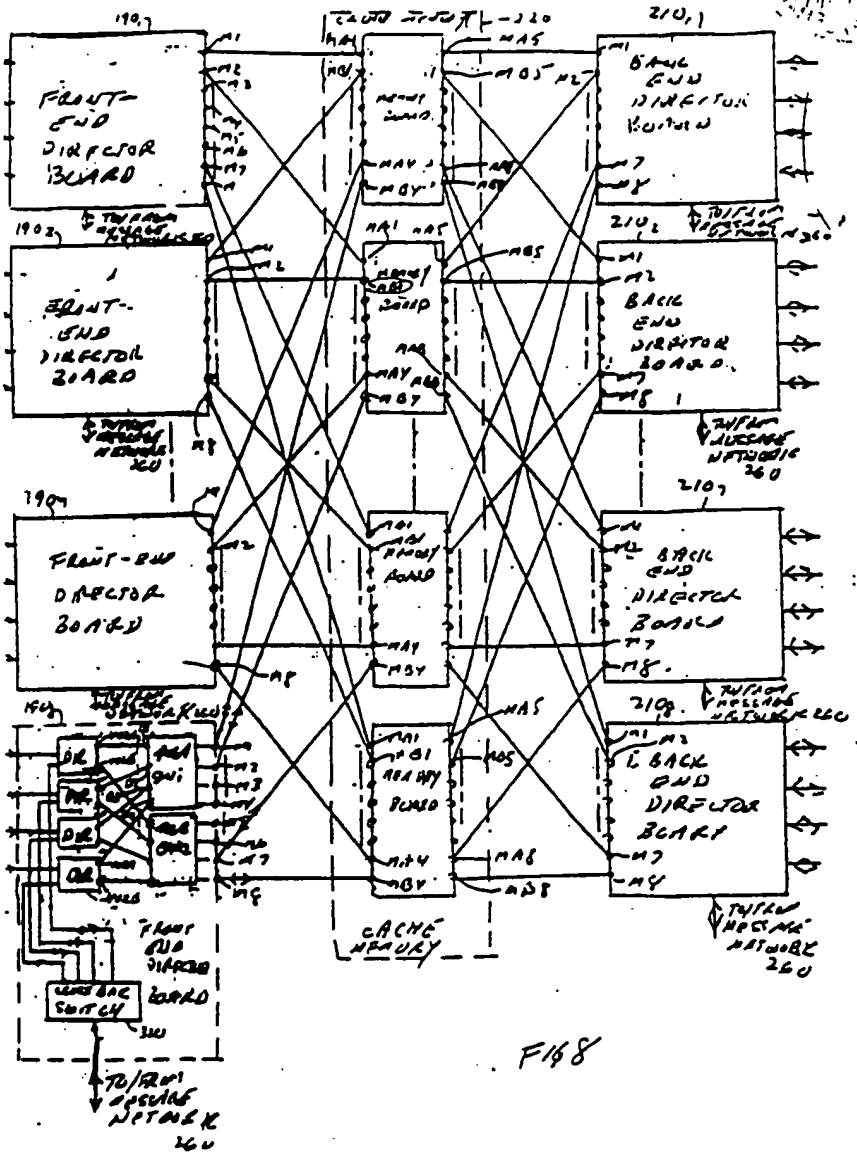

FRONT-END DIRECTOR BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
FRONT END DIRECTOR BOARD
SWITCH

Fig 8

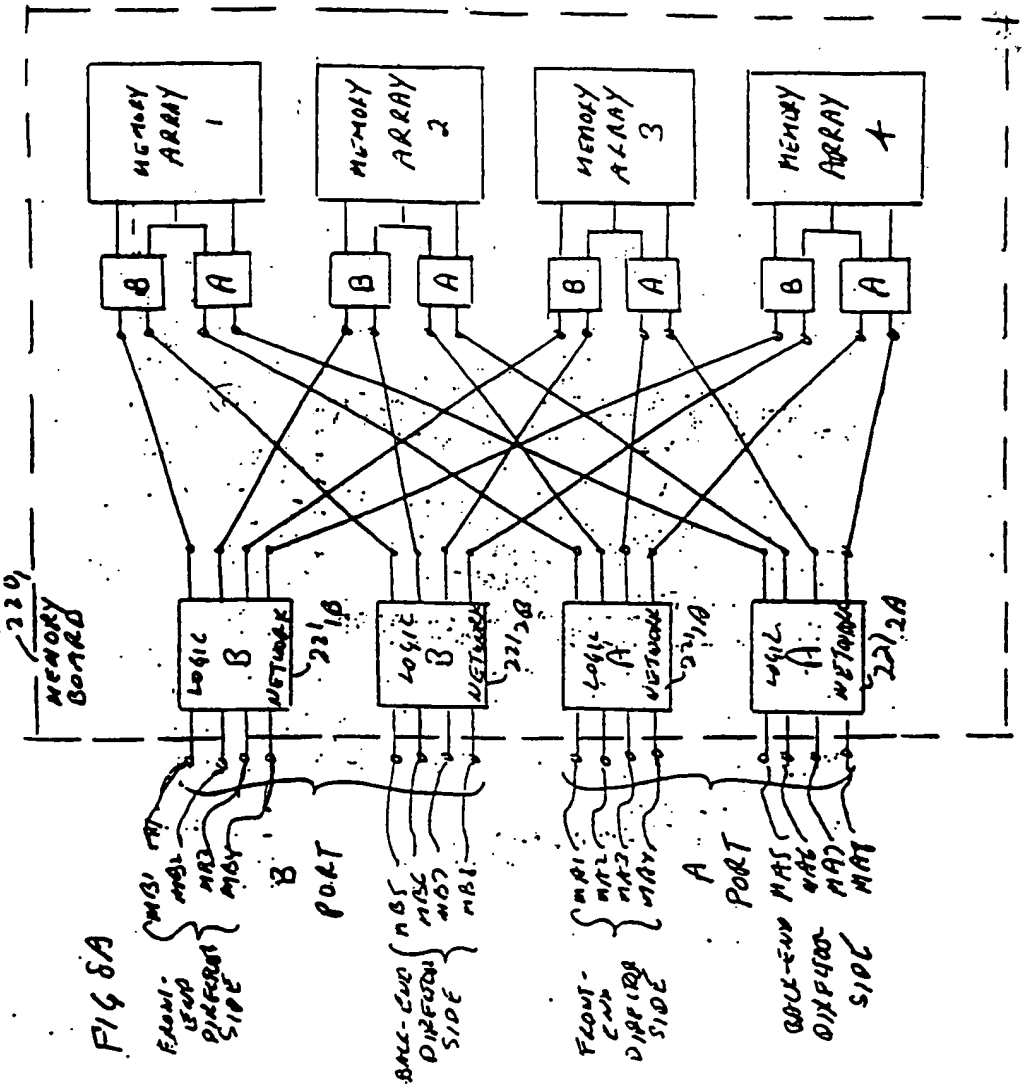

MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4
B
A
220
MEMORY BOARD
LOGIC B NETWORK
221B
LOGIC B NETWORK
221B
LOGIC A NETWORK
221A
LOGIC A NETWORK
221A
B PORT
A PORT
FRONT-END DIRECTOR SIDE
BACK-END DIRECTOR SIDE
FRONT-END DIRECTOR SIDE
BACK-END DIRECTOR SIDE

FIG 8A

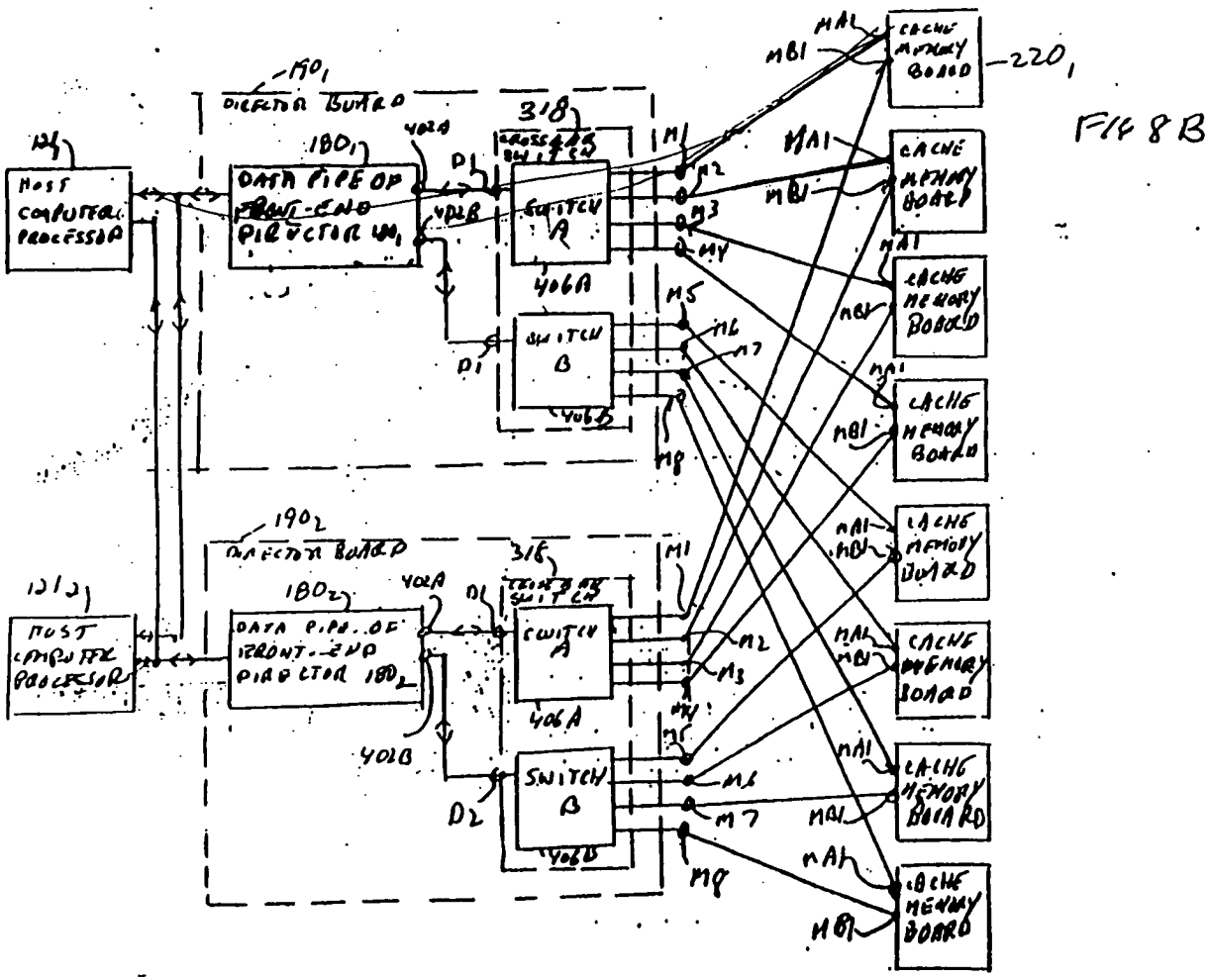


FIG 8B

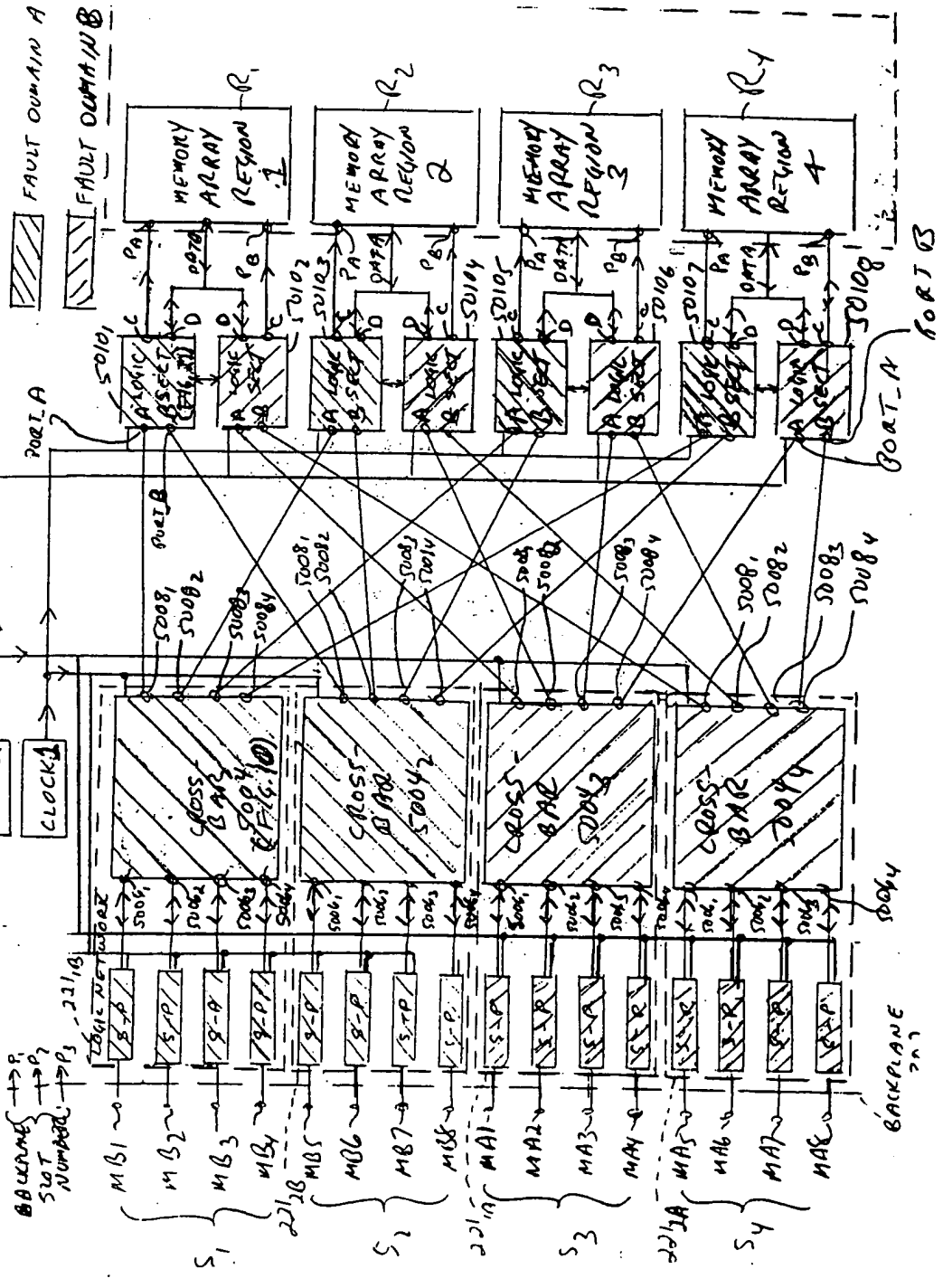

FAULT DOMAIN A
FAULT DOMAIN B
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
PORT_A
PORT_B
CLOCK2
CLOCK1
CROSS BAR SUBSYSTEM
BACKPLANE

FIG. 9

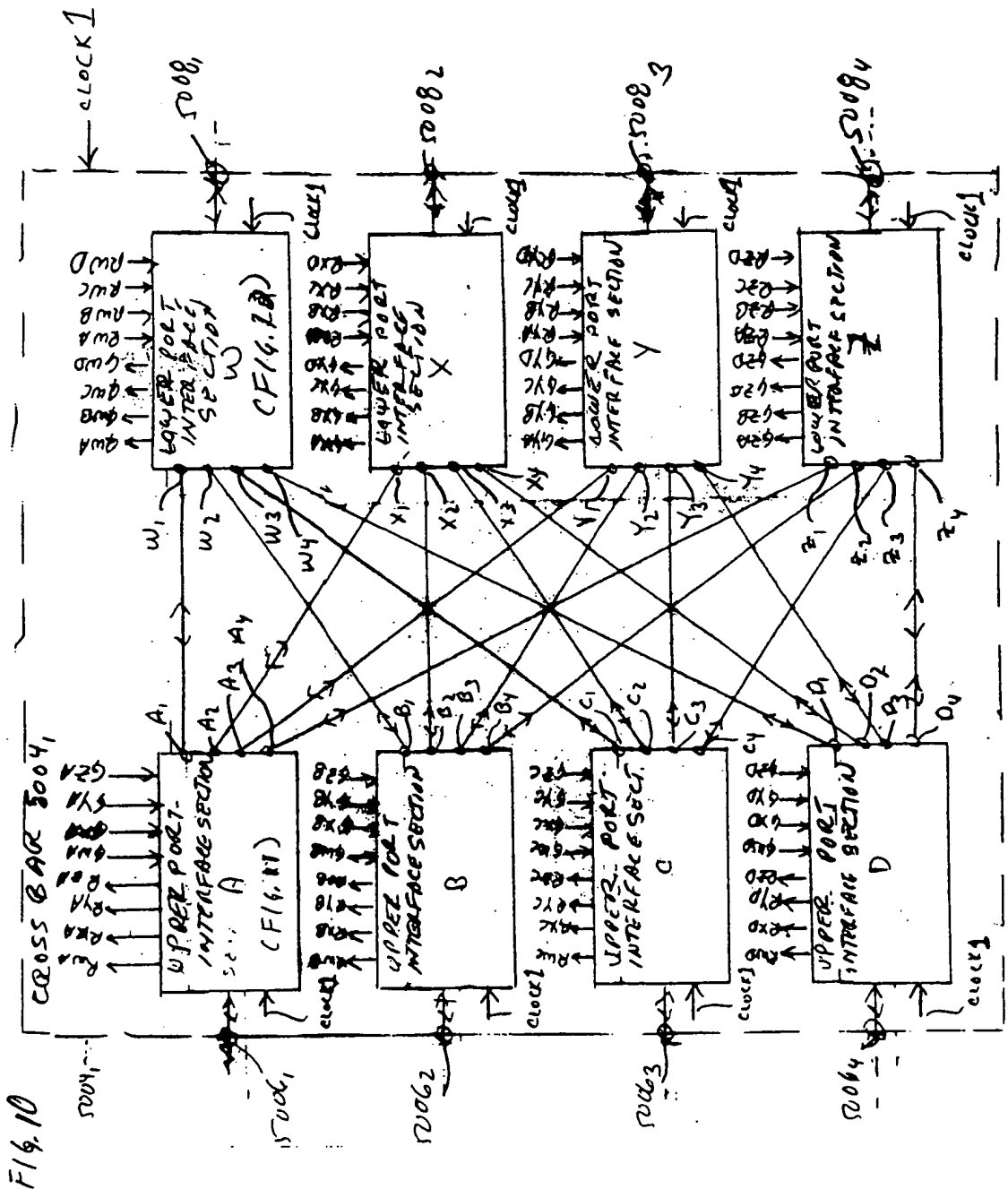

CROSS BAR 3004
UPPER PORT INTERFACE SECTION A
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECTION C
UPPER PORT INTERFACE SECTION D
LOWER PORT INTERFACE SECTION W
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
CLOCK 1
CLOCK 2
CLOCK 3
CLOCK 4

FIG. 10

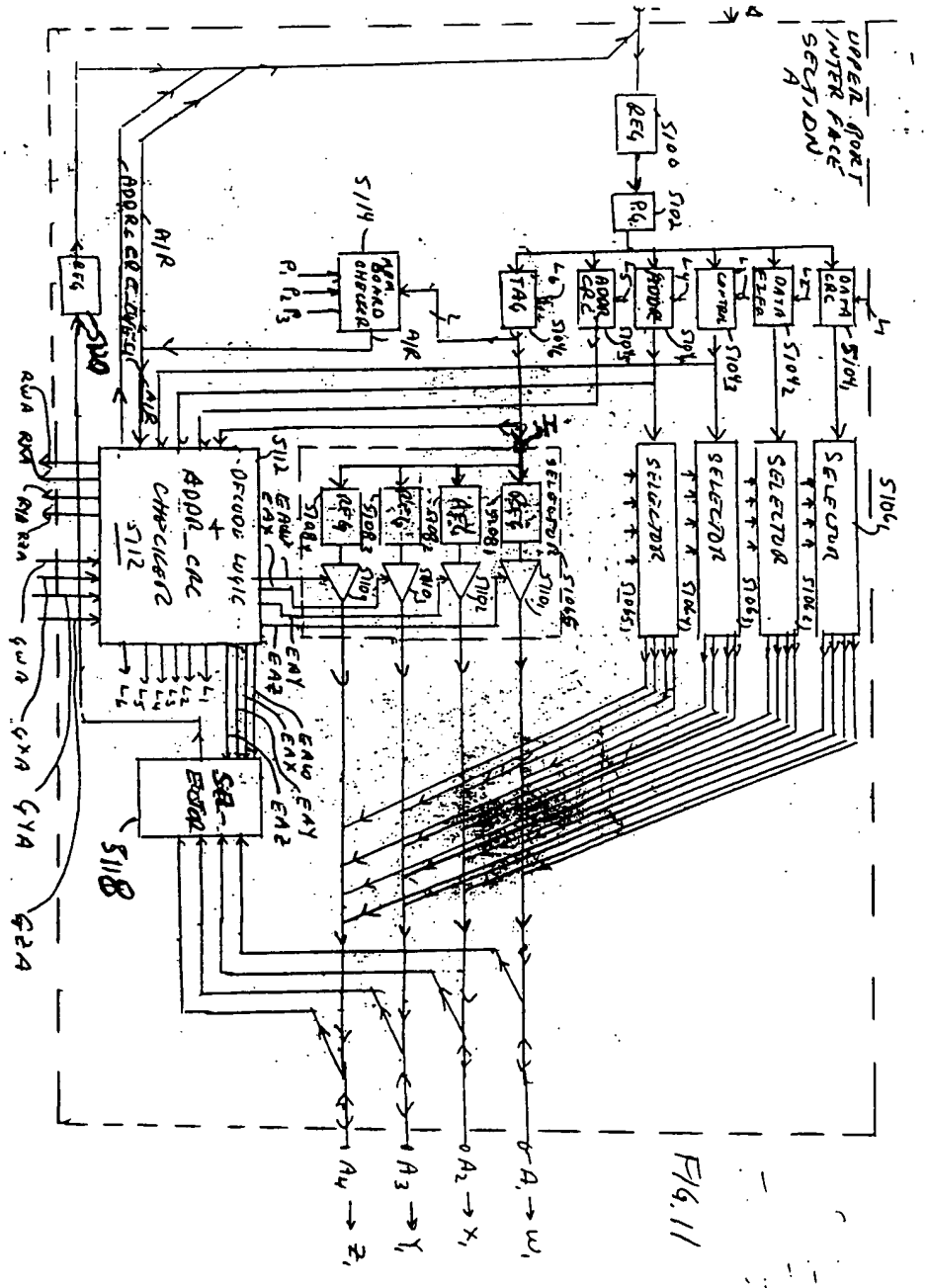

UPPER PORT INTER FACE SELECTION A
REG
PG
S100
S102
S114
HAMMING CHECKER
P1 P2 P3
ADDR
ADDR CRC
TAG
CONTROL
DATA FIELD
DATA CRC
S104
S106
S108
S110
S112
S116
S118
SELECTOR
SELECTOR STAGE
DECODE LOGIC + ADDR_CRC CHECKER
SEL DECOD
A1 → W1
A2 → X1
A3 → Y1
A4 → Z1

FIG. 11

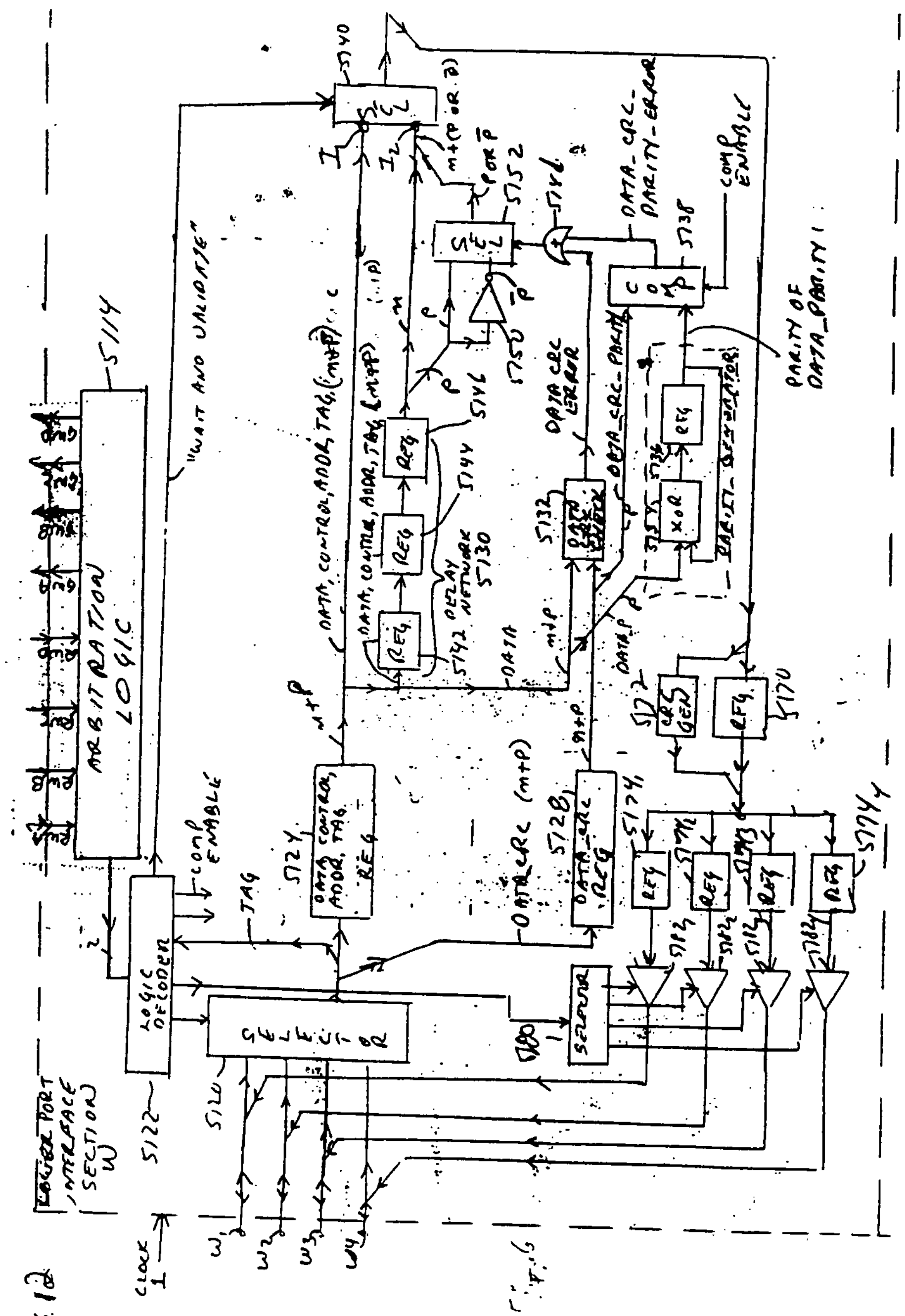
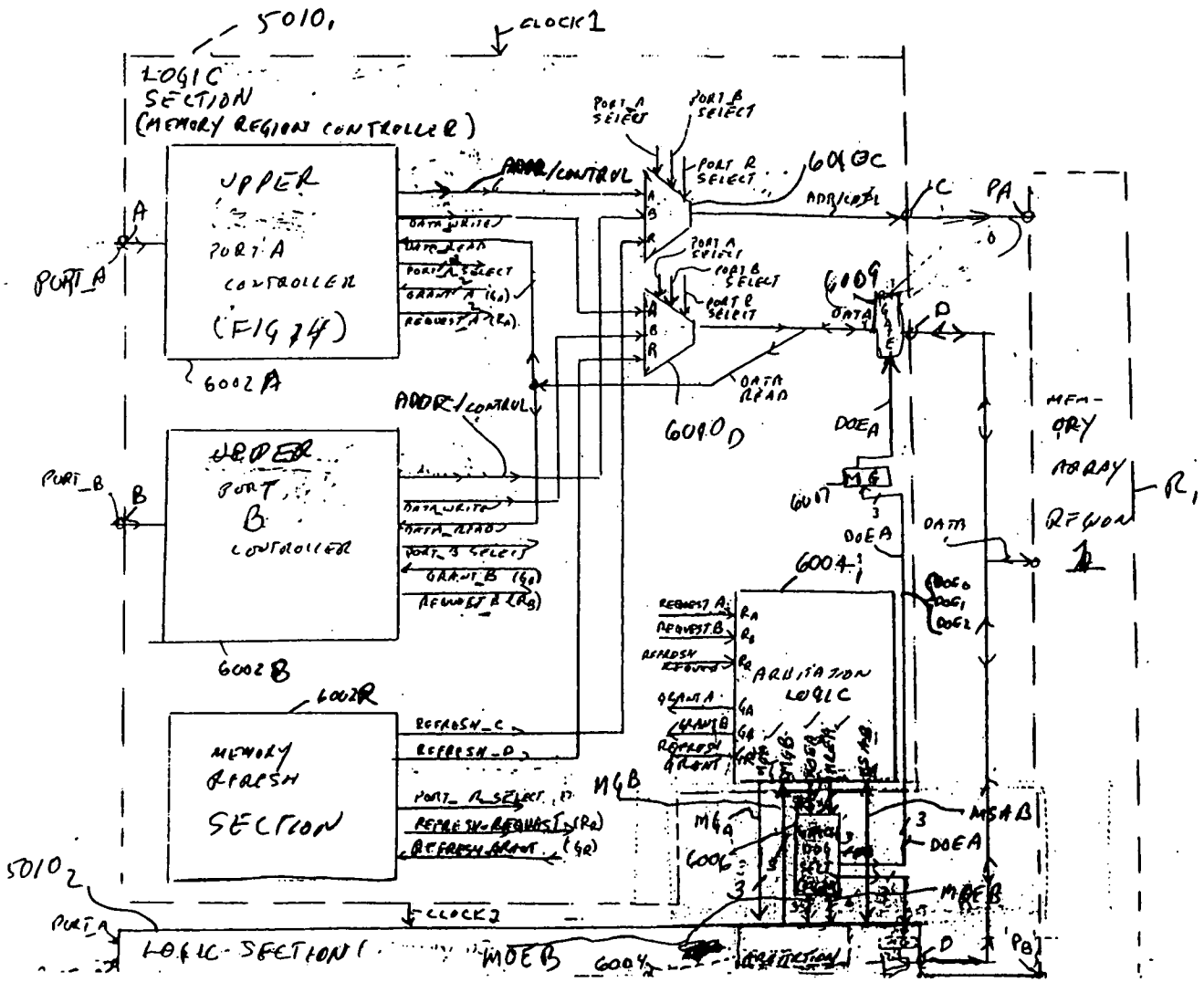
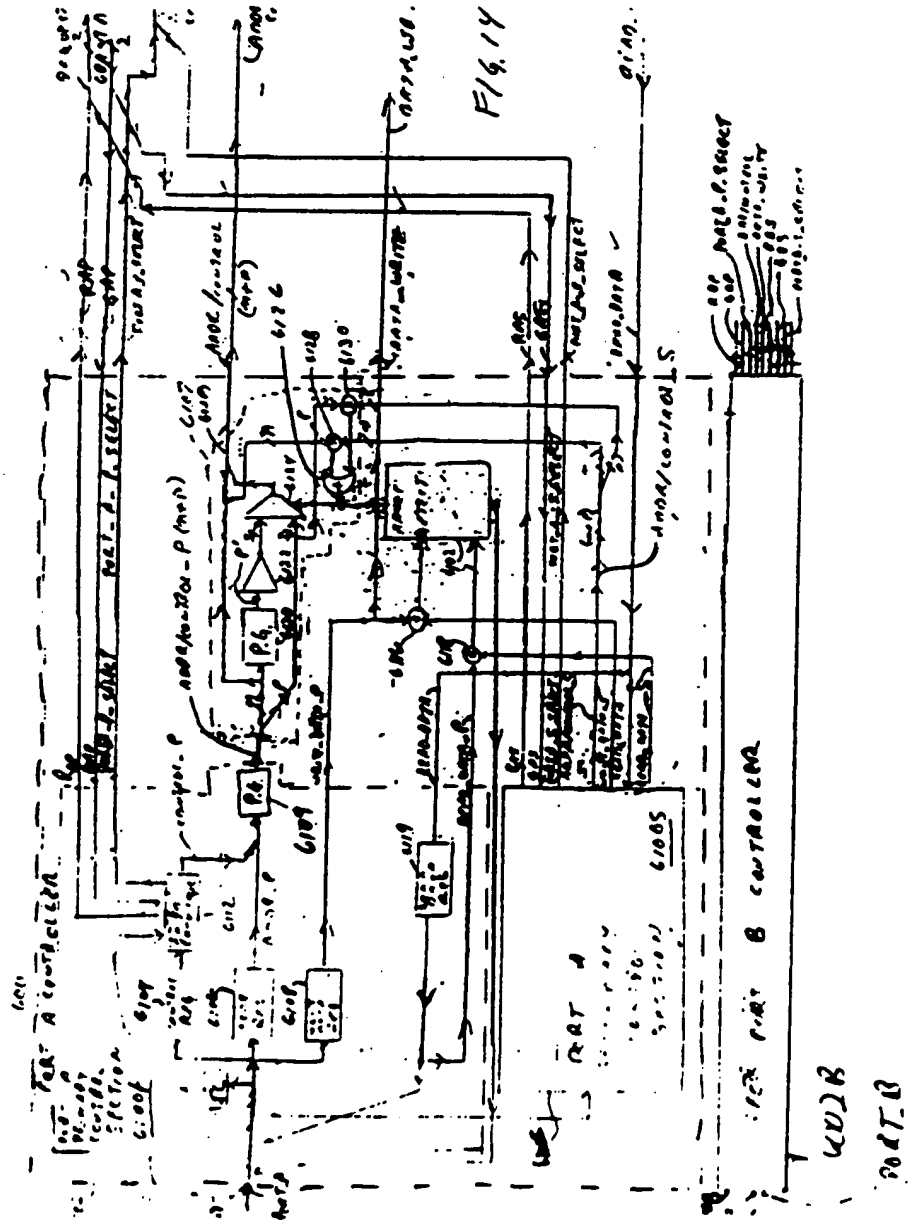

ARBITRATION LOGIC
LOGIC DECODER
SELECTOR
DATA, CONTROL, ADDR, TAG, REG
DATA CRC REG
DELAY NETWORK
DATA CRC ERROR
COMP ENABLE
PARITY GENERATOR
PARITY OF DATA_PARITY
DATA_CRC_PARITY_ERROR
"WAIT AND VALIDATE"
LOWER PORT INTERFACE SECTION W

FIG 12

FIG. 13





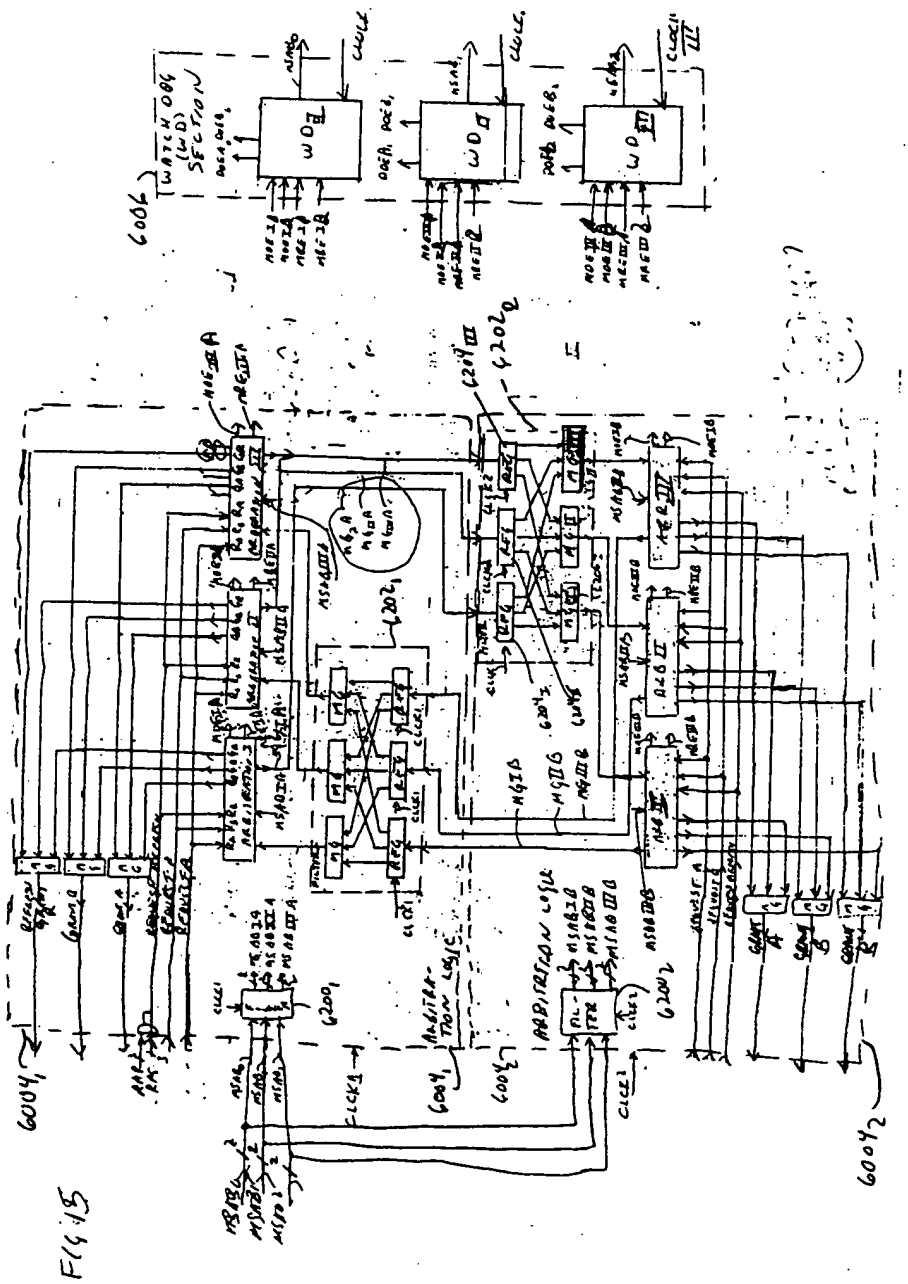


Fig. 7B

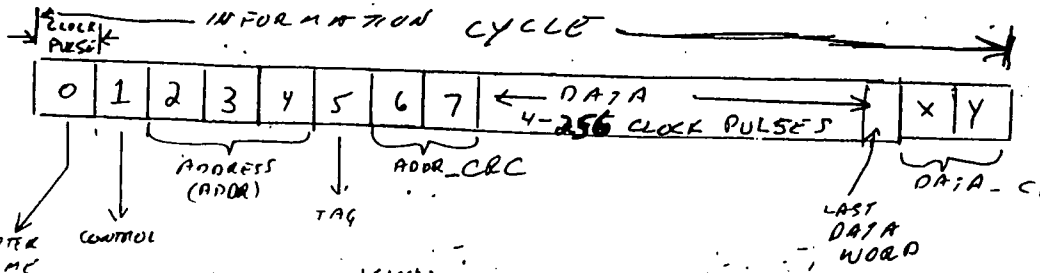


FIG. 16

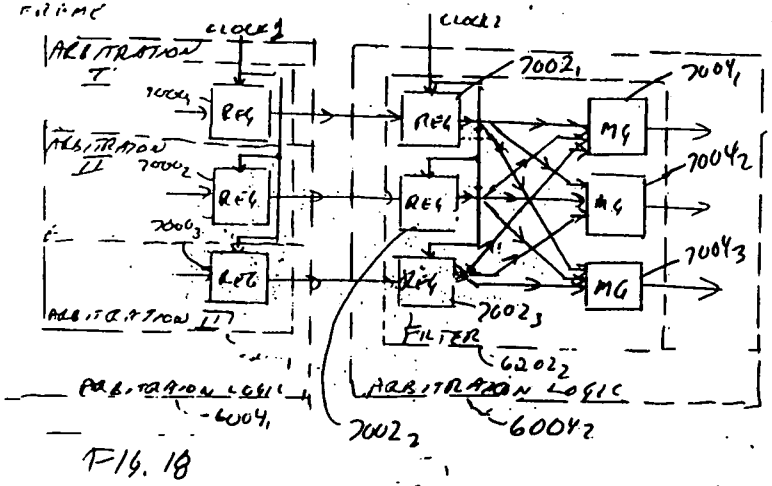


FIG. 18

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

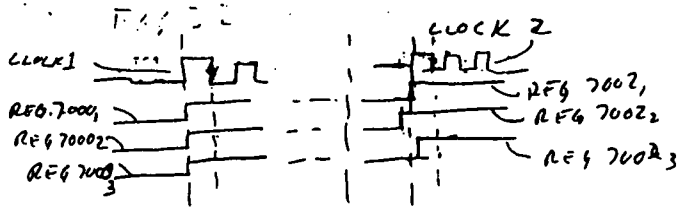
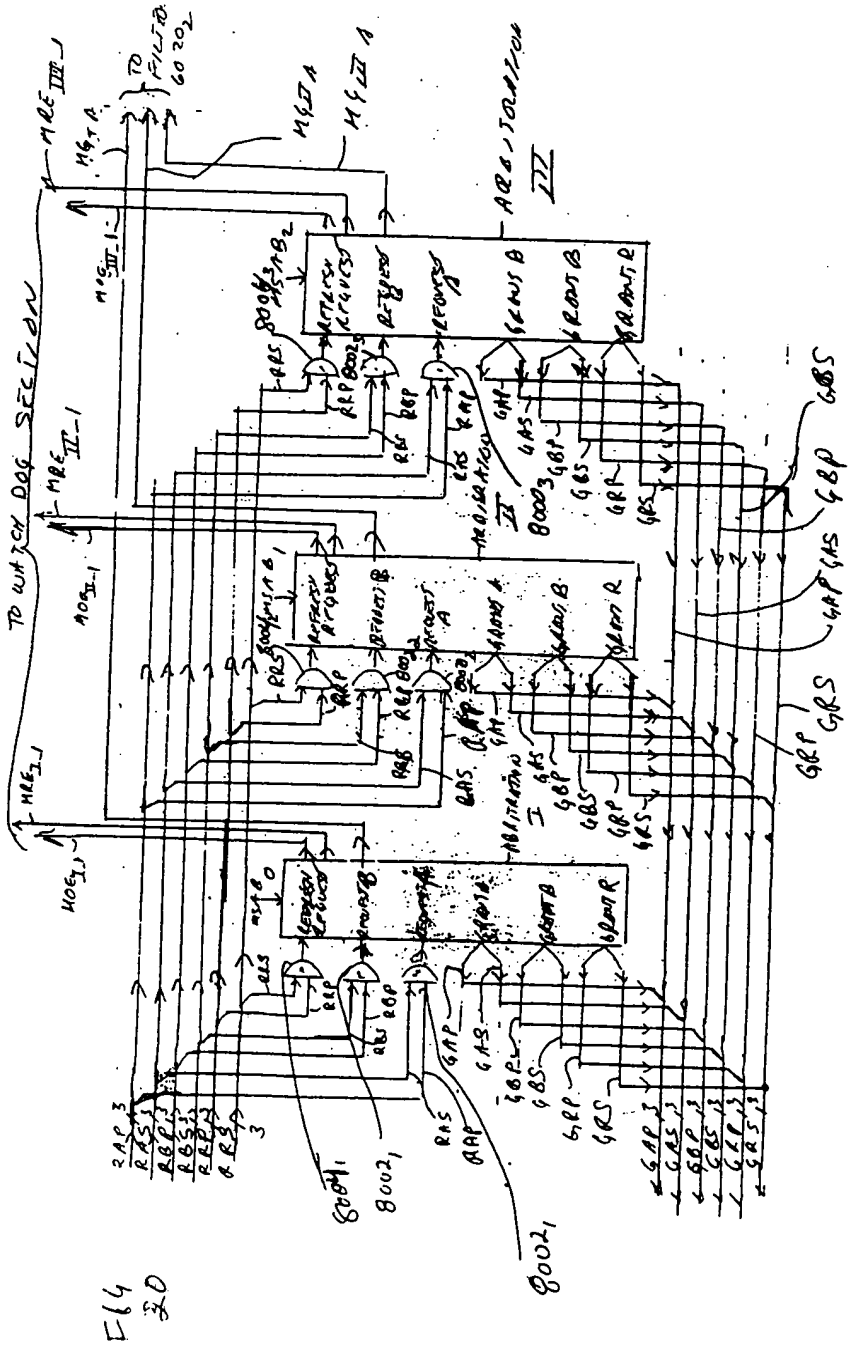


FIG. 19


TO WATCH DOG SELECTOR
MUX III
MUX II
MUX I
MUX 0
TO FIELD 60 202
MUX A
MUX B
ADDRESS COMPARATOR III
ADDRESS COMPARATOR II
ADDRESS COMPARATOR I
ADDRESS COMPARATOR 0
GAP
GBP
GAS
GBS
GRP
GRS
8002